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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,515	11/24/2003	Kenji Yamamoto	016891-0862	1969

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/718,515	YAMAMOTO, KENJI	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/718,515 filed on 11//24/2003. Claims 1 – 10 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 3, change "wirings' to —**wiring**—.
Claim 1, line 5, before "form" delete —**the**—.
Claim 1, line 8, change "said clock wiring" to —**each of said clock wirings**—.
Claim 1, line 8, before "clock buffers" insert —**plurality of**—.
Claim 1, line 10, change "wiring layer" to —**clock wiring**—.
Claim 1, line 12, after "switches" insert —**said clock wiring**—.
Claim 2, line 2, change "claims 1" to —**claim 1**—.
Claim 3, line 2, change "claims 1" to —**claim 1**—.
Claim 3, line 3, before "said selectors" insert —**each of**—.
Claim 3, line 3, change "select" to —**selects**—.
Claim 4, line 5, before "clock output" delete —**the**—.
Claim 4, line 5 – 6, change "the clock buffer" to —**a clock buffer**—.
Claim 4, line 11, change "the clock input" to —**a clock input**—.
Claim 4, line 11 – 12, change "the clock buffer" to —**a clock buffer**—.
Claim 4, line 15, delete —**and**—.
Claim 9, line 2, change "claims 4" to —**claim 4**—.
Claim 10, line 1, delete —**for master slice**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Applicant's Admitted Prior Art* (called *AAPA* hereinafter) in view of U.S. Patent No. 6,421,816 B1 to *Ishikura*.

5. As to Claim 1, *AAPA* (Specifications, pp. 1 – 7; Fig. 1; Fig. 2) shows and discloses the following subject matter:

- A master slice semiconductor integrated circuit (IC) comprising at *least two wiring layers* for wiring and a plurality of clock buffers connected by clock wirings in form of a clock three at least two cascaded stages to distribute clocks to a plurality of sequential circuits – [Specification, page 2, line 25 – page 7, line 27; Fig. 1; Fig. 2].

AAPA does not disclose that each of the clock wirings among the plurality of clock buffers comprises a *wiring layer switching portion* which switches a clock wiring between a lower wiring layer and an upper wiring layer. But *Ishikura* shows and teaches installing a *bridge wiring* 1403 close to input terminal of inverter 1402 along an wiring interconnected between inverter 1402 and inverter 1401 in order to suppress *antenna damage* to the inverter 1402 – [Fig. 9B; col. 18, line 60 – col. 20 line 9]. As illustrated in Fig. 9B, the *bridge wiring* 1403 is a *wiring layer switch portion*, it switches a wiring between inverter 1401 and inverter 1402 between a lower wiring layer and an upper wiring layer. Notice that *Ishikura* also teach that the *bridge wiring* can also be implemented to suppress *antenna damage* to a buffer in a semiconductor device (e.g., semiconductor IC) – [abstract].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Ishikura* in installing a *bridge wiring* (*wiring layer switching portion*) close to input terminal of each clock buffer in each clock wiring in order to suppress *antenna damage* thereby protecting each clock buffer in the master slice semiconductor IC..

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 10, reasons are included in **[Response A]**given above.

7. As to Claim 2, *Ishikura* teaches that the upper layer wiring and lower layer wiring of a *bridge wiring* is interconnected by *via-electrodes* (i.e., *via wirings*) – [col. 20, line 32 – 39].

For reference purposes, the explanations given above in response to Claim 2 are called **[Response B]** hereinafter.

8. As to Claim 3, *AAPA* shows the subject matter in Fig. 2.

9. As to Claim 4, reasons are included in **[Response A]** and **[Response B]** given above. In addition, *Ishikura* shows and teaches that the upper wiring layer is a wiring layer for customized wirings, and the low wiring layer is a wiring layer for fixed wirings – [Fig. 15(a); Fig. 15(b); Fig. 15(c); Fig. 15(d)].

10. As to Claims 5 and 6, *Ishikura* shows and teaches that the subject matter in Fig. 9A and **[Response B]** given above.

11. As to Claims 7 and 8, *Ishikura* shows and teaches that the subject matter in [Fig. 15(a); Fig. 15(b); Fig. 15(c); Fig. 15(d)] and **[Response B]** given above.

Allowable Subject Matter

12. Claim 9 is objected to as being dependent upon a rejected base claim, but it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 9 is allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- The master slice semiconductor integrated circuit according to Claim 4 further comprises a wiring which has a dummy load capacity equivalent to a load capacity connected to the input side via wiring in combination with other limitations as recited in **Claim 9**.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
September 27, 2005